# Alex Bashara

alexbashara2002@gmail.com ♦ 402-699-1326 ♦ LinkedIn ♦ GitHub

#### **EDUCATION**

**lowa State University, College of Engineering** Ames, Iowa Bachelor of Science in Computer Engineering

Expected December 2024 GPA 3.3/4.0

#### **EMPLOYMENT**

### Georgia Tech Research Institute

Applied Embedded Systems Engineer

Atlanta Georgia May 2023 – August 2023

- Developed VHDL code for FPGA based phased array radar systems used to track low orbit satellites
- Used AMD's Vivado to create hardware designs on a Xilinx Zyng RFSoC FPGA
- Collected incoming radar signals using ADCs and sent out radar signals using DACs
- Utilized data sampling techniques such as oversampling and decimation to reduce analog noise
- Created system design documentation used to present official system specifications to the customer

# Western Digital

Rochester, Minnesota

Enterprise SSD Firmware Engineer Co-op

May 2022 - December 2022

- Developed new SSD simulation software in Python for error injection, read/write simulation, and validation
- Standardized simulation software inputs using JSON files to specify run configurations
- Used FPGAs as test platforms to test firmware changes and new code features
- Helped create documentation for new simulation features to train other engineers
- Developed Python scripts to communicate with enterprise SSDs over UART to manipulate test drives
- Helped manage and update C flags in CMake build files
- Used software such as Jira to manage projects and report project progress

## **DESIGN PROJECT EXPERIENCE**

# Cyclone Racing Formula SAE

Electrical Team Lead

January 2023 - Present

- Lead a team of 10 engineers to create hardware, firmware, and software to meet team requirements
- Utilized CMSIS standard to interface with SMT32 ARM Cortex-M microcontrollers
- Focused on creating embedded C software libraries for ADC, CAN, SPI, LoRaWAN, and UART peripherals
- Implemented a FreeRTOS based telemetry system which has allowed for better real-time performance
- Setup a VSCode based development environment using ST-Tools and a GDB server
- · Created Makefiles to streamline building and development of the C codebase
- Validated the stability and reliability of software and identified issues using root cause analysis
- Managed and designed a custom microcontroller interface board using Altium Designer
- Assisted in developing and testing EV powertrain components and planning related control systems

## Microcontroller Engineer

June 2021 - May 2023

- Developed the first ever Cyclone Racing real-time wireless data acquisition system
- Wrote and debugged C code to interface with sensors and optimize wireless bandwidth on an AVR platform
- Utilized interfaces such as I2C, SPI, CAN, and UART to communicate between sensors and microcontrollers
- Designed PCBs in Altium for basic circuits such as sensor boards and LED shift lights
- Used oscilloscopes, signal generators, and power supplies to test and debug circuits and PCBs
- Simulated circuits in LTSpice and built circuits on breadboards for testing

### **MIPS VHDL Processor**

CprE 381 – Computer Architecture and Design

- Implemented a single cycle, software pipelined, and hardware pipelined VHDL CPU that supports MIPS ISA
- Created MIPS Assembly programs used to test the processor design and evaluate performance
- Created digital logic elements, control units, register files, forwarding units, and hazard detection hardware
- Used QuestaSim to simulate processor logic, evaluate program waveforms, and debug issues
- Wrote assembly benchmarks to analyze metrics such as CPI and clock frequency across architectures

#### **FPGA Based NES Emulator**

CprE 488 – Embedded Systems Design

- Used a Xilinx FPGA running ARM IP cores to create an NES emulator
- Developed using the Xilinx Vivado and Vitus environments to program VHDL hardware and C software
- Wrote software to create scaled images to output over the configured VGA interface
- Used Internal Logic Analyzer cores and an Oscilloscope to monitor internal signals and debug system issues
- Addressed memory mapped peripherals to configure a VDMA as well as interface with on board controls